IN THE SPECIFICATION

On page 2 at line 1, before the heading "BACKGROUND OF THE INVENTION" please insert the following:

A1

This application is a divisional of prior application serial no. 08/159,461 filed on November 30, 1993.

IN THE CLAIMS

Please cancel claims 1-16, 24 and 26-45 without prejudice. Please amend the remaining claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

sub B1 A2

17. (amended) A method of fabricating a portion of a semiconductor device comprising:

forming a gate structure on a substrate by:

depositing an insulating oxide layer on the substrate;

depositing a nitride layer on the oxide layer; and

depositing a polysilicon layer on the nitride layer; and

reoxidizing the gate structure to form a layer of oxide over the gate structure.

A2 cont'd
sub 01 cont'd

18. (amended) The method of claim 17, wherein the depositing step includes depositing the nitride layer on the insulating oxide layer to a thickness from about 10 Å to about 50 Å.

19. (unchanged) The method of claim 17, wherein the reoxidizing step includes reoxidizing the gate structure to form an oxide layer from about 25 Å to about 500 Å thick.

A3

20. (amended) The method of claim 17, further comprising:

patterning the gate structure by selectively etching away portions of the insulating oxide, nitride and polysilicon layers to expose a portion of the substrate and form a peripheral edge around the gate structure; and

exposing the substrate to an oxidizing ambient during reoxidation to oxidize the exposed portion of the substrate.

21. (amended) The method of claim 20, wherein the reoxidation causes an uplift in a peripheral portion of the nitride layer.

22. (amended) The method of claim 20, wherein the reoxidation causes an indentation in the substrate near the peripheral edge of the gate structure.

A3 cont'd

23. (amended) The method of claim 17, further comprising:

prior to the reoxidizing step, forming source and drain regions in the substrate.

25. (amended) A method for fabricating a portion of a semiconductor device, comprising:

A4

forming an oxide gate layer on a surface of a substrate;

forming a nitride layer on the oxide gate layer by depositing the nitride layer on the oxide gate layer;

forming a polysilicon layer on the nitride layer;

patterning the polysilicon and nitride layers to form a gate structure; and

reoxidizing the gate structure to form a layer of oxide over the gate structure and on sidewalls of the gate structure.

46. (unchanged) An integrated circuit device comprising:

a substrate;

a gate structure, wherein the gate structure includes:

a gate oxide layer on the substrate,

a nitride layer on the gate oxide layer, and

a polysilicon layer over the nitride layer;

a channel region under the gate structure; and

source/drain regions in the substrate adjacent the channel region.

47. (unchanged) The integrated circuit device of claim 46, wherein the nitride layer is from about 10 Å to about 50 Å thick.

48. (unchanged) The integrated circuit device of claim 46, wherein the nitride layer is deposited over said gate oxide layer.

49. (unchanged) The integrated circuit device of claim 46, wherein the nitride layer is formed by nitrogen implantation to form an implanted area and by annealing of the implanted area.

50. (amended) The integrated circuit device of claim 46, wherein the gate structure has a peripheral edge and further including an uplift in portions of the nitride layer proximate the peripheral edge of the gate structure, the uplift caused by reoxidation of the gate structure, wherein asperities are absent from the polysilicon layer.

51. (amended) The integrated circuit device of claim 46, wherein the substrate has a surface and further including an indentation in the surface of the substrate located proximate to the peripheral edge of the gate structure, the indentation resulting from reoxidation of the gate structure.

52. (amended) The integrated circuit device of claim 46 further wherein the gate structure includes sidewall spacers located on each edge of the gate structure and lightly doped drain regions in the substrate below the sidewalls spacers.

53. (unchanged) The integrated circuit device of claim 46, wherein the substrate is a p-type substrate and wherein the source/drain regions are formed by implanting n-type impurities in the p-type substrate.

54. (unchanged) The integrated circuit device of claim 53, wherein the source/drain regions are implanted prior to reoxidation.

55. (unchanged) The integrated circuit device of claim 53, wherein the source/drain regions are implanted after oxidation.

Please add the following new claims:

--56. (newly added) The integrated circuit device of claim 46, wherein the channel region has a length not greater than 0.8 μm.

57. (newly added) The integrated circuit device of claim 46, wherein the gate oxide layer is not greater than 200 Å thick.

58. (newly added) The method of claim 23, wherein a channel region beneath the gate structure between the source/drain regions has a length not greater than 0.8 μm.

59. (newly added) The method of claim 25, further comprising:

forming the oxide gate layer to a thickness not greater than 200 Å.--